REMARKS

Claims 1, 2 and 4-11 are pending. By this Amendment, claim 1 is amended to better distinguish over the prior art. Furthermore, claim 3 is canceled without prejudice to or disclaimer of the subject matter contained therein. Reconsideration is respectfully requested.

It is gratefully appreciated that the Office Action indicates that claims 2 and 6-8 are allowed.

The Office Action rejects claims 1, 4 and 5 under 35 U.S.C. §103(a) over Hayashi (U.S. Publication No. 2003/0197598); Brown (U.S. Patent No. 6,417,526) and Streetman ("Solid State Electronic Devices"); and claim 3 under 35 U.S.C. §103(a) over Hayashi, Brown, Streetman and Kanbara (U.S. Patent No. 4,575,925). Claim 3 is canceled. Thus, the rejection of this claim is moot. However, the rejections as applied to remaining claims are respectfully traversed.

In particular, the applied references do not disclose or suggest a semiconductor device, including at least a diode, the diode including a p-type silicon layer, the p-type silicon layer containing germanium, and an n-type silicon layer junctioned to the p-type silicon layer and the n-type silicon layer being disposed on an insulting layer, as recited in independent claim 1.

Specifically, Hayashi discloses an IC card 1 that includes a semiconductor integrated circuit 2.

Brown discloses in Figure 1 a semiconductor body 10 that includes a p-conductivity region that includes a mixed crystal of silicon and germanium. See column 5, lines 25-35.

Streetman discloses solid state electronic devices including switching diodes.

Kanbara discloses a method for fabricating a connection to a deep buried layer of a bi-polar transistor based on SOI technology.

In contrast to the claimed invention, none of the applied references disclose or suggest a semiconductor device, including at least a diode, the diode including a p-type silicon layer, the p-type silicon layer containing germanium, and an n-type silicon layer junctioned to the p-type silicon layer and the n-type silicon layer being disposed on an insulting layer. On the contrary nowhere in the applied references are these features disclosed or suggested.

Thus, any combination of the applied references would not have resulted in a device having a lateral structure whereby the diode is reduced more effectively compared to a stacked diode as shown in Brown. Accordingly, because it would not have been obvious to combine the applied references to arrive at the claimed invention, it is respectfully requested that the rejections under 35 U.S.C. §103(a) be withdrawn.

In view of the foregoing, this application is in condition for allowance. Favorable reconsideration and prompt allowance of the claims are earnestly solicited.

Should the Examiner believe that anything further is desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact Applicant's attorney at the telephone number listed below.

Respectfully submitted,

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Attachment:
Request for Continued Examination

Date: June 30, 2005

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